ONE-TRANSISTOR FLOATING-BODY DRAM CELL IN BULK CMOS PROCESS WITH ELECTRICALLY ISOLATED CHARGE STORAGE REGION

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RELATED APPLICATIONS

[0001] The present invention is a divisional of U.S. Patent Application Serial No. 10/095,901 filed March 11, 2002, now U.S. PATENT No. 6,661,042, and is related to commonly owned, co-filed U.S. Patent Application Serial No. 10/095,984 filed March 11, 2002, now U.S. PATENT No. 6,686,624.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a dynamic random access memory (DRAM) cell, as well as methods for operating and fabricating a DRAM cell. More specifically, the present invention relates to a one-transistor floating-body DRAM cell formed using a process compatible with a bulk CMOS process, wherein charge is stored inside an electrically isolated body region underneath the transistor channel region.

Related Art

[0003] Conventional one-transistor, one-capacitor (1T/1C) DRAM cells require a complex process for fabrication. Moreover, significant area is required to form the capacitor needed for storage of signal charge. Recently, one-transistor, floating-body (1T/FB) DRAM cells using partially-depleted silicon-on-insulator (PD-SOI) processes have been proposed, in which a signal charge is stored inside a floating body region, which modulates the threshold voltage (V_T) of the transistor. As a result, the separate capacitor of a 1T/FB DRAM cell can be eliminated, thereby resulting in reduced cell area and higher density. Periodic refresh operations are still required for these 1T/FB DRAM cells to counteract the loss of stored charge